

EL465782903US

MI56305686

EV026160720US

EL169866954

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

* * * *

**Method Of Depositing Polysilicon, Method Of
Fabricating A Field Effect Transistor, Method Of
Forming A Contact To A Substrate, Method Of
Forming A Capacitor**

* * * *

INVENTORS

Michael Nuttall
Er-Xuan Ping
Yongjun Jeff Hu

ATTORNEY'S DOCKET NO. MI22-821

~~Ansatz~~
METHOD OF DEPOSITING POLYSILICON, METHOD OF
FABRICATING A FIELD EFFECT TRANSISTOR, METHOD OF
FORMING A CONTACT TO A SUBSTRATE, METHOD OF
FORMING A CAPACITOR

TECHNICAL FIELD

This invention relates to methods of depositing polysilicon, to methods of fabricating field effect transistor, to methods of forming contacts to substrates and to methods of forming capacitors.

BACKGROUND OF THE INVENTION

Device geometry continues to shrink in semiconductor circuitry fabrication. For example, field effect transistor gate width is now commonly below one micron and source/drain junction depth 1000 Angstroms or less. A challenge in such constructions is to reduce parasitic source/drain serial resistance while maintaining low source/drain diode leakage. Such resistance can be reduced by providing a thicker salicide over the source/drain. Such is typically provided by depositing a metal layer on the source/drain which typically comprises monocrystalline silicon. A subsequent anneal causes a reaction which consumes a portion of the silicon to form the silicide. However, large consumption of silicon to form the desired thicker salicide results in the salicide/junction interface being very close to the base of the junction.

1 This causes source/drain diode leakage current to the substrate to
2 increase.

3 Raised or elevated source/drain constructions in field effect
4 transistors can be utilized to minimize or reduce the amount of silicon
5 consumed in forming a silicide portion of a substrate contact. Further,
6 raised source/drain constructions can provide desired field effect
7 transistor constructions independent of the silicide contact which is
8 typically formed. For example, raised source/drain transistors are
9 commonly used in logic device applications where device speed is an
10 important factor.

11 Elevated source/drain constructions are typically formed in the
12 prior art by selectively growing epitaxial monocrystalline silicon atop the
13 silicon junction regions. Such is typically accomplished in costly
14 epitaxial reactors operating under ultra high vacuum (UHV), for example
15 at vacuum pressures of the order of 0.001 mTorr. Violette et al., "Low
16 temperature selective silicon epitaxy by ultra high vacuum rapid thermal
17 chemical vapor deposition using Si_2H_6 , H_2 and Cl_2 ", Applied Physics
18 Letter 68(1), pp.66-68, January 1, 1996 disclose a selective epi silicon
19 deposition process occurring at 800°C and 30mTorr or less.

20 It would be desirable to improve upon these and other prior art
21 processes of selectively forming silicon over silicon substrates. Although
22 motivated from this objective, the artisan will appreciate other
23 applicability of the disclosed technology, with the invention only being

1 limited by the accompanying claims appropriately interpreted in
2 accordance with the Doctrine Of Equivalents.

3

4

5 **SUMMARY OF THE INVENTION**

6 In but one aspect of the invention, a method of depositing
7 polysilicon comprises providing a substrate within a chemical vapor
8 deposition reactor, with the substrate having an exposed substantially
9 crystalline region and an exposed substantially amorphous region. A
10 gaseous precursor comprising silicon is fed to the chemical vapor
11 deposition reactor under conditions effective to substantially selectively
12 deposit polysilicon on the crystalline region and not the amorphous
13 region.

14 In another aspect a method of fabricating a field effect transistor
15 on a substrate comprises forming a gate dielectric layer and a gate over
16 semiconductive material. Doped source/drain regions are formed within
17 semiconductive material laterally proximate the gate. Substantially
18 amorphous insulating material is formed over and laterally proximate the
19 gate. The substrate is provided within a chemical vapor deposition
20 reactor. A gaseous precursor comprising silicon is fed to the chemical
21 vapor deposition reactor under conditions effective to substantially
22 selectively deposit polysilicon on the source/drain regions and not on

1 substantially amorphous material, and forming elevated source/drains on
2 the doped source/drain regions.

3 In but another aspect, a method of forming a contact to a
4 substrate comprises forming substantially amorphous insulating material
5 over a substrate node location. A contact opening is etched through
6 the amorphous insulating material over the node location. The node
7 location is provided to comprise an outwardly exposed substantially
8 crystalline surface. The substrate with outwardly exposed substantially
9 crystalline node location surface is provided within a chemical vapor
10 deposition reactor. A gaseous precursor comprising silicon is fed to the
11 chemical vapor deposition reactor under conditions effective to
12 substantially selectively deposit polysilicon on the outwardly exposed
13 crystalline node location surface and not on the insulating material.

14 An aspect of the invention also comprises forming a capacitor.
15 In one implementation, a substrate is provided within a chemical vapor
16 deposition reactor. The substrate has an exposed substantially crystalline
17 region and an exposed substantially amorphous region. A gaseous
18 precursor comprising silicon is fed to the chemical vapor deposition
19 reactor under conditions effective to substantially selectively deposit
20 polysilicon on the crystalline region and not the amorphous region, and
21 the polysilicon is formed into a first capacitor electrode. A capacitor
22 dielectric layer is formed over the polysilicon. A second capacitor
23 electrode is formed over the capacitor dielectric layer.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic view of a semiconductor wafer fragment at one process in accordance with the invention.

Fig. 2 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that depicted by Fig. 1.

Fig. 3 is an alternate view of the Fig. 1 wafer fragment at an alternate processing step subsequent to that depicted by Fig. 1.

Fig. 4 is a diagrammatic view of an alternate embodiment semiconductor wafer fragment at a processing step in accordance with an aspect of the invention.

Fig. 5 is a view of the Fig. 4 wafer fragment at a processing step subsequent to that shown by Fig. 4.

Fig. 6 is a diagrammatic sectional view of yet another alternate embodiment wafer fragment at a processing step in accordance with an aspect of the invention.

Fig. 7 is a diagrammatic sectional view of still another alternate embodiment wafer fragment at a processing step in accordance with an aspect of the invention.

Fig. 8 is a view of the Fig. 7 wafer fragment at a processing step subsequent to that shown by Fig. 7.

Fig. 9 is yet another view of an alternate embodiment semiconductor wafer fragment at a processing step in accordance with an aspect of the invention.

Fig. 10 is a view of the Fig. 9 wafer fragment at a processing step subsequent to that depicted by Fig. 9.

Fig. 11 is a view of the Fig. 9 wafer fragment at a processing step subsequent to that depicted by Fig. 10.

Fig. 12 is a view of the Fig. 9 wafer fragment at a processing step subsequent to that depicted by Fig. 11.

Fig. 13 is still another view of an alternate embodiment semiconductor wafer fragment at a processing step in accordance with an aspect of the invention.

Fig. 14 is a view of the Fig. 13 wafer fragment at a processing step subsequent to that depicted by Fig. 13.

Fig. 15 is a view of the Fig. 13 wafer fragment at a processing step subsequent to that depicted by Fig. 14.

JM B3 17
18
19
20
21
22
23
24

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

In the prior art, polysilicon is typically deposited by chemical vapor deposition utilizing precursor gases, such as silane. Typical deposition temperatures are from 500°C to 625°C at a pressure ranging from 50 mTorr to 1 Torr. Deposition temperatures less than about 550°C result in an amorphous deposition while deposition temperatures greater than 550°C result in a polycrystalline deposition. Regardless, the deposition typically results in a uniform, conformal layer of silicon atop the semiconductor substrate.

Referring to Fig. 1, a semiconductor wafer in process is indicated generally with reference numeral 10. Such comprises, for example, a bulk monocrystalline silicon substrate 12 having an exposed insulating dielectric layer or region 14 associated therewith, such as SiO₂ or Si₃N₄. Monocrystalline silicon 12 presents an exposed substantially crystalline region 16, while all of the illustrated dielectric material 14 constitutes an exposed substantially amorphous dielectric material region as depicted in Fig. 1. In the context of this document, "substantially crystalline" and "substantially amorphous" refer to the respective attributes at greater than 90% of the exposed material at its exposed surface. For example, an exposed substantially crystalline region will

have its exposed surface having at least 90% crystallinity, while an exposed substantially amorphous region will have its exposed surface being at least 90% amorphous. Also in the context of this document, "predominately" means greater than 50%.

Further in the context of this document, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

Referring to Fig. 2, wafer 10 is provided within a chemical vapor deposition reactor. Preferably, the wafer has been subjected to a native oxide strip, such as by using an HF dip, immediately prior to placement with the reactor. A gaseous precursor comprising silicon is fed to the reactor under conditions effective to substantially selectively deposit a polysilicon layer 18 on crystalline region 16 and not on amorphous region 14. In the context of this document, "substantially selective" or "substantially selectively" denotes deposition over one region as compared to another to a thickness ratio of greater than 5:1. An example and preferred reactor is a hot wall low pressure chemical vapor deposition reactor, with the processing conditions being void of plasma generation.

1 Alternately, plasma can be utilized. Exemplary and suitable conditions
2 within the reactor comprise a temperature of greater than or equal to
3 about 650°C and a pressure less than or equal to about 100 mTorr.
4 A preferred upper temperature limit is 850°C. Also preferably, pressure
5 is greater than 30 mTorr and temperature is less than 800°C during
6 deposition, thus overcoming the extreme low pressure/high temperature
7 environments (and thus costs associated therewith) of the prior art
8 epitaxial silicon deposition processes. Accordingly in one implementation,
9 the invention enables use of conventional, lower cost deposition furnaces
10 instead of the ultra high vacuum rapid thermal epi reactors.

11 Example preferred silicon precursors include silanes, including
12 chlorosilanes. Specific examples include SiH₄, Si₂H₆, and SiCl₂H₂.
13 However most preferably, the deposition conditions are void of feeding
14 chlorine containing gas to the reactor thus eliminating any tendency of
15 the substrate being etched during the selective deposition. The
16 invention was reduced to practice utilizing a vertical hot wall LPCVD
17 reactor holding 100 wafers. The feed gas was SiH₄ at 50 sccm, with
18 the atmosphere within the reactor during processing consisting entirely
19 or essentially of such gaseous silane precursor. Temperature during
20 processing was 700°C, with pressure being substantially maintained at
21 70 mTorr. An exemplary broader range for gas flow is from about
22 20 sccm to about 1000 sccm. Under such conditions, near 100%
23 selectivity in the deposition was achieved (i.e., essentially no deposition

over region 14) during deposition of the first 1500 Angstroms of polysilicon. Above this thickness, polysilicon began to deposit on region 14, which comprised undoped SiO₂. Modifying process conditions by one or both of raising temperature and lowering pressure will have greater improvement on selectivity as a function of thickness. Regardless, such reduction-to-practice example conditions in the subject reactor do have significant utility, as present and future generations of semiconductor wafer fabrication comprises deposition of polysilicon layers to less than 1000 Angstroms.

sub B4 ▶ Alternate exposed crystalline surfaces, by way of example only, utilizable in the context of the invention include silicides (such as TiSi_x and WSi₄), crystalline dielectrics (such as barium strontium titanate and Ta₂O₅), aluminum, copper, aluminum-copper alloys, tungsten, and other crystalline metals or metal-like materials. Selectivity in the deposition is expected to be greatest where the reactor atmosphere during the time period of deposition is substantially void of a gas comprising a conductivity enhancing dopant, or other gases, although conductivity enhancing gases (such as B₂H₆) are expected to provide functional selectivity in accordance with the invention. →

An alternate considered embodiment is described with reference to Fig. 3 which illustrates a semiconductor wafer fragment 10a. Like numerals from the first described embodiment are utilized where appropriate, with differences being indicated with the suffix "a" or with

1 different numerals. In this example, materials 12a (and correspondingly
2 exposed region 16a) and 14a can be considered as presenting exposed
3 predominately crystalline and predominately amorphous regions,
4 respectively. Such regions could also constitute exposed substantially
5 crystalline and substantially amorphous regions, respectively. Within a
6 chemical vapor deposition reactor, a gaseous silicon precursor is fed
7 under conditions effective to deposit a polysilicon layer 18a on both the
8 exposed crystalline and amorphous regions. Polysilicon layer 18a has a
9 region 19 within the previously exposed at least predominately crystalline
10 region 16a and a region 20 over the exposed at least predominately
11 amorphous region. Deposited polysilicon region 19 has a greater
12 thickness than deposited polysilicon region 20. Region 20 can be
13 subsequently removed if desired.

14 In accordance with the reduction to practice example, such was
15 achieved with a silane flow rate at 50 sccm with reactor temperature
16 and pressure during processing being maintained at 700°C and
17 70 mTorr, respectively, when the thickness of region 18a reached about
18 1500 Angstroms. In such reduction-to-practice example, exposed
19 region 16a was substantially crystalline and region 14a was substantially
20 amorphous. Modifying deposition conditions by one or both of lowering
21 temperature and raising pressure will result in lowering of the threshold
22 thickness upon which appreciable deposition begins relative to the
23 exposed amorphous region. Further, modifying crystalline/amorphous

content of the exposed surface(s) by reducing the degree of crystallinity below 90% in region 16a and reducing amorphous content to below 90% in region 14a would further impact by lowering the threshold thickness limit where appreciable polysilicon begins to develop on the exposed predominately amorphous region.

The invention can have applicability, for example, in fabrication of field effect transistors, such as will now be described with reference to Figs. 4 and 5. Fig. 4 illustrates a semiconductor wafer fragment 24 comprised of a bulk monocrystalline silicon substrate 26 having isolation regions 28 formed therein. A gate construction 30 is provided centrally between isolation regions 28. Such comprises a gate dielectric layer 32 and a gate 34 provided thereover. Gate 34 preferably comprises a silicide layer over a polysilicon layer. Substantially amorphous insulating material, such as Si_3N_4 in the illustrated form of anisotropically etched sidewall spacers 36 and cap 38, is provided over and laterally proximate gate 34, with the illustrated gate construction 30 being provided over semiconductive material 26. Doped source/drain regions 40 and 42 are formed within semiconductive material 26 laterally proximate the illustrated gate.

Referring to Fig. 5, wafer 24 has been provided within a chemical vapor deposition reactor and processed as described above effectively to substantially selectively deposit polysilicon on source/drain regions 40 and 42, and not on the substantially amorphous material of regions 28,

36 and 38. Elevated source/drain regions 44 and 46 are formed on
doped source/drain regions 40 and 42, respectively. An example and
preferred thickness for the entirety of each region 40/44, and 42/46 is
500 Angstroms. As an alternate example, doping to fully form
regions 40 and 42 could occur after provisions of elevated regions 44
and 46.

Fig. 6 illustrates exemplary alternate processing relative to a wafer
fragment 24a. Like numerals from the Figs. 4 and 5 embodiment are
utilized where appropriate, with differences being indicated with a
suffix "a", or with different numerals. Wafer fragment 24a is the same
as that depicted in Fig. 4, and additionally includes formation of a
substantially amorphous insulating material layer 48 (for example such
as SiO_2 , doped or undoped, or Si_3N_4) thereover. Openings 50 and 52
have been etched through amorphous insulating material layer 48 over
the illustrated source/drain regions to expose such regions, while leaving
the gate protectively covered with amorphous insulating material.
Processing would then continue as described above with respect to
Fig. 5, with the elevated source/drain regions forming as described above
(not shown in Fig. 6). Such processing might be desired where other
portions of the wafer are desired to be masked during the substantially
selective polysilicon deposition, or where polysilicon growth is desired on
less than all of the exposed source/drain regions or other crystalline
material regions which would be exposed but for provision of layer 48.

Further exemplary processing is next described with reference to Figs. 7 and 8 relative to a wafer fragment 60. Such comprises a crystalline substrate 62 having a conductive diffusion region 64 formed therein. In this example, the crystalline silicon is monocrystalline silicon, but other substrates could be utilized where the node location of interest is polycrystalline silicon. Region 64 constitutes a substrate node location to which electrical contact is desired. A substantially amorphous insulating material layer 66 is formed over substrate node location 64, and a contact opening 68 is etched through such material over node location 64, and in this example, all the way to the crystalline silicon of node location 64.

Referring to Fig. 8, substrate 60 has been provided within a chemical vapor deposition reactor and processing conducted, as for example as described above, effectively to substantially selectively deposit polysilicon 70 within contact opening 68 on crystalline silicon of node location 64, and not on insulating material 66.

Further alternate processing is described with reference to Figs. 9-12 with respect to a semiconductor wafer fragment 72. Like numerals from the first described embodiment have been utilized where appropriate with differences being indicated with the suffix "a" or with different numerals. Wafer fragment 72 appears as wafer fragment 60 of Fig. 7 at a processing step immediately subsequent thereto.

100500E-045102

1 Specifically, wafer fragment 72 includes a deposited metal layer 74, such
2 as Ti or W.

3 Referring to Figs. 10 and 11, wafer fragment 72 has been
4 subjected to, for example, conventional SALACIDE processing to form
5 a silicide region 76 at the base of contact opening 68. Metal layer 74
6 is thereafter stripped (Fig. 11) to leave silicide region 76 at the base
7 of contact 68. Such provides a node location at the base of
8 contact 68 which, in this example, comprises an outwardly exposed
9 substantially crystalline surface in the form of a silicide.

10 Referring to Fig. 12, wafer fragment 72 has been provided within
11 a chemical vapor deposition reactor and conditions provided to be
12 effective to substantially selectively deposit polysilicon 80 on the
13 outwardly exposed silicide node location surface and not on insulating
14 material 66.

15 Further alternate processing is next described with reference to
16 Figs. 13-15 regarding methods of forming a capacitor. Fig. 13 illustrates
17 a semiconductor wafer fragment 81 comprised of bulk monocrystalline
18 silicon 82 having a diffusion region 83 formed therein. A layer of
19 amorphous silicon dioxide 84 is formed thereover. A contact
20 opening 86 is etched through layer 84 to diffusion region 83.
21 Opening 86 is plugged with a crystalline material 87, such as conductive
22 polysilicon, and planarized relative to layer 84.
23
24

Referring to Fig. 14, substrate 81 has been placed within a chemical vapor deposition reactor and processed as described above to selectively deposit polysilicon 88 over crystalline material 87. Polysilicon 88 can be further processed, such as by patterning, to form a desired first capacitor electrode shape if the initial deposition is not as desired.

MURB5 Referring to Fig. 15, a capacitor dielectric layer 89 is deposited followed by deposition of a second capacitor electrode layer 90 to form a capacitor 93. Such can be formed by conventional or other processing. For example, techniques of the invention as described above can be utilized to selectively deposit second capacitor electrode layer 90 on dielectric layer 89 where such is fabricated to be crystalline. For example, barium strontium titanate and Ta_2O_5 are exemplary crystalline capacitor dielectric layer materials. Such material can be deposited over first capacitor electrode 88, patterned if desired to provide exposed amorphous material and the crystalline material 89 where desired, and a selective deposition as described above then conducted.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or

modifications within the proper scope of the appended claims
appropriately interpreted in accordance with the doctrine of equivalents.

PATENT OFFICE

1

2 modifications within the proper scope of the appended claims
3 appropriately interpreted in accordance with the doctrine of equivalents.

4

5

6

8

9

10

11

12

13

14

15

16

17

18

19

20

21

22

23

24